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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,874	08/10/2004	Rajat CHAUHAN	TI-38154	4873

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EXAMINER	
TRAN, ANH Q	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,874	CHAUHAN ET AL.	
	Examiner	Art Unit	
	Anh Q. Tran	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *5-16* is/are allowed.

6)☒ Claim(s) *1-4 and 17-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/12/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Whitworth (6,556,040).

Claim 1, Whitworth shows a method of reducing the effect of coupling on a reference signal (311 and 313) due to a transition in an output signal (308) generated by an output buffer (316 and 202) on an output path, said method being performed in said output buffer, said method comprising:

inverting (326) said output signal to generate an inverted signal (330); and

connecting said inverted signal through an impedance (332 and 334) that stores an energy, said inverted signal being connected to a node (322 and 312) at which said reference signal is received by said output buffer.

Claim 2, Whitworth shows the method of claim 2, wherein said impedance comprises a capacitor (332 and 334).

Claim 4, Whitworth shows the method of claim 2, wherein a capacitance of said capacitor equals (col. 6, lines 15-18) the parasitic capacitance of a transistor (316) connected between said node and said output path, said transistor being comprised in said output buffer.

3. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Maley et al. (5,969,542).

Claim 1, Maley shows a method of reducing the effect of coupling on a reference signal (IN) due to a transition in an output signal (OUT_LSP) generated by an output buffer (10, Fig. 3) on an output path, said method being performed in said output buffer, said method comprising:

inverting (P101) said output signal to generate an inverted signal (OUTB_LSP); and

connecting said inverted signal through an impedance (C2) that stores an energy, said inverted signal being connected to a node (at N102 gate) at which said reference signal (IN is received by transistor N102 which is part of the buffer) is received by said output buffer.

Claim 2, Maley shows the method of claim 2, wherein said impedance comprises a capacitor (C2 is a capacitor).

Claim 3, Maley shows the method of claim 2, wherein said output buffer is implemented using transistors (N102, N104, P104, P102) of a voltage specification of a first voltage level (VDD-2 volt), said output signal is generated having a swing equaling a second voltage level (VDDIO-3.3 volt), wherein said first voltage level is lower than said second voltage level (col. 4, lines 41-45).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 17, 18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ko (6,218,854) in view of Whitworth (6,556,040).

Claim 17, Ko shows an apparatus comprising: an input interface module (200, Fig. 8A) providing an interface to receive an input signal (A); an output interface module (116) providing the output signal on an output node (B). Ko discloses the claimed invention except for a processing logic generating said output signal in response to said input signal, said processing logic comprising: means for generating an inverted signal based on said output signal; and means for connecting said inverted signal through an impedance that Stores an energy, said inverted signal being connected to a node at which said reference signal is received.

However, Whitworth shows a processing logic (300, Fig. 3) generating said output signal (308) in response to said input signal (306), said processing logic comprising: means (326) for generating an inverted signal based on said output signal; and means (332 and 334) for connecting said inverted signal through an impedance that Stores an energy, said inverted signal being connected to a node (322 and 312) at which said reference signal (311 and 313) is received.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace processing logic (110, Fig. 8A) of Ko with the processing logic of Whitworth, in order to provide appropriate clamping signal and stabilizing a clamping transistor control node by way of capacitor.

Claim 18, Whitworth shows the apparatus of claim 17, wherein said impedance comprises a capacitor (332 and 334).

Claim 20, Whitworth shows apparatus of claim 18, wherein a capacitance of said capacitor equals (col. 6, lines 15-18) the parasitic capacitance of a transistor (316) connected between said node and said output path, said transistor being comprised in said output buffer.

6. Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (6,392,439) in view of Maley et al. (5,969,542).

Claim 17, Tanaka shows an apparatus comprising: an input interface module (601, Fig. 14) providing an interface to receive an input signal (in0 and in0b); an output interface module (602) providing the output signal (OUT0) on an output node (inherent limitation); a processing logic (6031) generating the output signal. Tanaka discloses the claimed invention except for the processing logic comprising: means for generating an inverted signal based on said output signal; and means for connecting said inverted signal through an impedance that Stores an energy, said inverted signal being connected to a node at which said reference signal is received.

However, Maley shows the processing logic (10, Fig. 3) comprising: means (P101) for generating an inverted signal (OUTB_LSP) based on said output signal

(OUT_LSP); and means (C2) for connecting said inverted signal through an impedance that Stores an energy, said inverted signal being connected to a node (a node at N102 gate) at which said reference signal (IN) is received.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to replace processing logic of Tanaka with the processing logic of Maley, in order to provide level shifter with higher speed of the transitions at the gates of the pair of cross-coupled P-channel transistors.

Claim 18, Maley shows the apparatus of claim 17, wherein said impedance comprises a capacitor (C2 is a capacitor).

Claim 20, Maley shows the apparatus of claim 18, wherein said output signal is generated by an output buffer on an output path, said output buffer is implemented using transistors (N102, N104, P104, P102 are implement with regular NMOS and PMOS which are the same as a core device, col. 41-45) of a voltage specification of a second voltage level (VDD-2), wherein said second voltage level is lower than said first voltage level (VDDIO-3.3 volt).

Allowable Subject Matter

7. Claims 5-16 are allowed.

8. The following is an examiner's statement of reasons for allowance: with respect to claims 5 and 12, in addition to other limitations in the claims, the prior art of record fails to teach, disclose, or render obvious the applicant's invention as claimed, particularly the feature describing:

-the gate terminal of the third transistor is coupled to a reference voltage at a first node, the drain terminal of the transistor is coupled to the drain terminal of the fourth transistor.

-a third transistor and a fourth transistor protecting said first transistor and said second transistor from exposure to said first voltage level, each of said third transistor and said fourth transistor containing a source terminal, a gate terminal and a drain terminal, the gate terminal of each of said third transistor and said fourth transistor being coupled to receive a reference signal, a parasitic capacitance of said third transistor and said fourth transistor coupling said output signal to said reference signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh Q. Tran whose telephone number is 571-272-1813. The examiner can normally be reached on M-F (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH Q. TRAN
PRIMARY EXAMINER

2/17/06